

What is claimed is:

1. A semiconductor device comprising:

a semiconductor chip having a first major surface and a second major surface facing opposite to the first major surface;

5 a first electrode layer on the first major surface;

a second electrode layer on the second major surface;

an active region in a vicinity of the first major surface, the active region being in electrical contact with the first electrode layer;

10 a layer with low electrical resistance of a first conductivity type in a vicinity of the second major surface, the layer with low electrical resistance being in electrical contact with the second electrode layer;

a drain drift region between the first major surface and the layer with low electrical resistance, the drain drift region providing a vertical drift current path in the ON-state of the semiconductor device, the drain drift region being depleted in the OFF-state of the

15 semiconductor device;

a third electrode layer above the first major surface with an insulation film interposed therebetween, an ON and OFF state of the semiconductor device being controlled through the third electrode layer, at least a part of the third electrode layer being in close proximity to the first electrode layer;

20 wherein the drain drift region comprises a first alternating conductivity type layer comprising vertically extending first semiconductor regions of the first conductivity type and vertically extending second semiconductor regions of a second conductivity type arranged alternately at a first pitch of repeating;

25 a breakdown withstanding region is located around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown withstanding region providing substantially no current path in the ON-state of the semiconductor device, the breakdown withstanding region being depleted in the OFF-state of the semiconductor device, the breakdown withstanding region comprising a second alternating conductivity type layer comprising vertically extending third semiconductor regions

of the first conductivity type and vertically extending fourth semiconductor regions of the second conductivity type arranged alternately at a second pitch of repeating;

an under region below the third electrode layer, the under region comprising a third alternating conductivity type layer comprising vertically extending fifth semiconductor regions of the first conductivity type and vertically extending sixth semiconductor regions of the second conductivity type arranged alternately at a third pitch of repeating; and

wherein the third pitch of repeating is narrower than the first pitch of repeating.

2. The semiconductor device according to Claim 1, wherein the third alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

3. A semiconductor device comprising:

a semiconductor chip having a first major surface and a second major surface facing opposite to the first major surface;

a first electrode layer on the first major surface;

a second electrode layer on the second major surface;

an active region in a vicinity of the first major surface, the active region being in electrical contact with the first electrode layer;

a layer with low electrical resistance of a first conductivity type in the vicinity of the second major surface, the layer with low electrical resistance being in electrical contact with the second electrode layer;

a drain drift region between the first major surface and the layer with low electrical resistance, the drain drift region providing a vertical drift current path in the ON-state of the semiconductor device, the drain drift region being depleted in the OFF-state of the

semiconductor device;

a third electrode layer above the first major surface with an insulation film interposed therebetween, an ON and OFF state of the semiconductor device being controlled through the

third electrode layer, at least a part of the third electrode layer being in close proximity to the first electrode layer;

wherein the drain drift region comprises a first alternating conductivity type layer comprising vertically extending first semiconductor regions of the first conductivity type and vertically extending second semiconductor regions of a second conductivity type arranged alternately at a first pitch of repeating;

a breakdown withstanding region around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown withstanding region providing substantially no current path in the ON-state of the semiconductor device, the breakdown withstanding region being depleted in the OFF-state of the semiconductor device, the breakdown withstanding region comprising a second alternating conductivity type layer comprising vertically extending third semiconductor regions of the first conductivity type and vertically extending fourth semiconductor regions of the second conductivity type arranged alternately at a second pitch of repeating;

an under region below the third electrode layer, the under region comprising a third alternating conductivity type layer comprising vertically extending fifth semiconductor regions of the first conductivity type and vertically extending sixth semiconductor regions of the second conductivity type arranged alternately at a third pitch of repeating; and

wherein the third alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

4. The semiconductor device according to Claim 1, wherein the second pitch of repeating is narrower than the first pitch of repeating.

5. The semiconductor device according to Claim 1, wherein the second pitch of repeating is narrower than the first pitch of repeating.

6. The semiconductor device according to Claim 1, wherein the second alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

7. The semiconductor device according to Claim 3, wherein the second alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

8. The semiconductor device according to Claim 1, further comprising a first well region of the second conductivity type connected electrically to the first electrode layer, the first well region covering the surface of the third alternating conductivity type layer on the side of the first major surface.

9. The semiconductor device according to Claim 3, further comprising a first well region of the second conductivity type connected electrically to the first electrode layer, the first well region covering the surface of the third alternating conductivity type layer on the side of the first major surface.

10. The semiconductor device according to Claim 8, wherein the surface of the third alternating conductivity type layer on the side of the first major surface is in contact with the bottom of the first well region.

11. The semiconductor device according to Claim 9, wherein the surface of the third alternating conductivity type layer on the side of the first major surface is in contact with the bottom of the first well region.

12. The semiconductor device according to Claim 1, wherein the first through sixth semiconductor regions of the first through third alternating conductivity type layers are shaped with respective stripes in a plane parallel to the first major surface or the second major surface.

5 13. The semiconductor device according to Claim 3, wherein the first through sixth semiconductor regions of the first through third alternating conductivity type layers are shaped with respective stripes in a plane parallel to the first major surface or the second major surface.

10 14. The semiconductor device according to Claim 12, wherein the pn-junctions in the second alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

15 15. The semiconductor device according to Claim 13, wherein the pn-junctions in the second alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

16. The semiconductor device according to Claim 12, wherein the pn-junctions in the second alternating conductivity type layer extend in perpendicular to the pn-junctions in the first alternating conductivity type layer.

20 17. The semiconductor device according to Claim 13, wherein the pn-junctions in the second alternating conductivity type layer extend in perpendicular to the pn-junctions in the first alternating conductivity type layer.

18. The semiconductor device according to Claim 12, wherein the pn-junctions in the third alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

5 19. The semiconductor device according to Claim 13, wherein the pn-junctions in the third alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

10 20. The semiconductor device according to Claim 12, wherein the pn-junctions in the third alternating conductivity type layer extend in perpendicular to the pn-junctions in the first alternating conductivity type layer.

15 21. The semiconductor device according to Claim 13, wherein the pn-junctions in the third alternating conductivity type layer extend in perpendicular to the pn-junctions in the first alternating conductivity type layer.

22. A semiconductor device comprising:
a semiconductor chip having a first major surface and a second major surface facing opposite to the first major surface;
20 a first electrode layer on the first major surface having a first peripheral portion;
a second electrode layer on the second major surface;
an active region in a vicinity of the first major surface, the active region being in electrical contact with the first electrode layer;
a layer with low electrical resistance of a first conductivity type in a vicinity of the second
25 major surface, the layer with low electrical resistance being in electrical contact with the second electrode layer;

a drain drift region between the first major surface and the layer with low electrical resistance, the drain drift region providing a vertical drift current path in the ON-state of the semiconductor device, the drain drift region being depleted in the OFF-state of the semiconductor device, wherein the drain drift region comprises a first alternating conductivity type layer comprising vertically extending first semiconductor regions of the first conductivity type and vertically extending second semiconductor regions of a second conductivity type arranged alternately at a first pitch of repeating;

a breakdown withstanding region around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown withstanding region providing substantially no current path in the ON-state of the semiconductor device, the breakdown withstanding region being depleted in the OFF-state of the semiconductor device, the breakdown withstanding region comprising a second alternating conductivity type layer comprising vertically extending third semiconductor regions of the first conductivity type and vertically extending fourth semiconductor regions of the second conductivity type arranged alternately at a second pitch of repeating;

an under region below the first peripheral portion of the first electrode layer, the under region comprising a third alternating conductivity type layer comprising vertically extending fifth semiconductor regions of the first conductivity type and vertically extending sixth semiconductor regions of the second conductivity type arranged alternately at a third pitch of repeating; and

wherein the third pitch of repeating is narrower than the first pitch of repeating.

23. The semiconductor device according to Claim 22, wherein the third alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

24. A semiconductor device comprising:

a semiconductor chip having a first major surface and a second major surface facing opposite to the first major surface;

a first electrode layer on the first major surface having a first peripheral portion;

a second electrode layer on the second major surface;

an active region in a vicinity of the first major surface, the active region being in electrical contact with the first electrode layer;

5 a layer with low electrical resistance of a first conductivity type in a vicinity of the second major surface, the layer with low electrical resistance being in electrical contact with the second electrode layer;

10 a drain drift region between the first major surface and the layer with low electrical resistance, the drain drift region providing a vertical drift current path in the ON-state of the semiconductor device, the drain drift region being depleted in the OFF-state of the semiconductor device, wherein the drain drift region comprises a first alternating conductivity type layer comprising vertically extending first semiconductor regions of the first conductivity type and vertically extending second semiconductor regions of a second conductivity type arranged alternately at a first pitch of repeating;

15 a breakdown withstanding region around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown withstanding region providing substantially no current path in the ON-state of the semiconductor device, the breakdown withstanding region being depleted in the OFF-state of the semiconductor device, the breakdown withstanding region comprising a second alternating conductivity type layer comprising vertically extending third semiconductor regions of the first conductivity type and vertically extending fourth semiconductor regions of the second conductivity type arranged alternately at a second pitch of repeating;

20 an under region below the first peripheral portion of the first electrode layer, the under region comprising a third alternating conductivity type layer comprising vertically extending fifth semiconductor regions of the first conductivity type and vertically extending sixth semiconductor regions of the second conductivity type arranged alternately at a third pitch of repeating; and

25 wherein the third alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

25. The semiconductor device according to Claim 22, wherein the first electrode layer further comprises a second peripheral portion, under which the second alternating conductivity type layer is extended.

5 26. The semiconductor device according to Claim 24, wherein the first electrode layer further comprises a second peripheral portion, under which the second alternating conductivity type layer is extended.

10 27. The semiconductor device according to Claim 22, wherein the second pitch of repeating is narrower than the first pitch of repeating.

28. The semiconductor device according to Claim 24, wherein the second pitch of repeating is narrower than the first pitch of repeating.

15 29. The semiconductor device according to Claim 22, wherein the second alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

30. The semiconductor device according to Claim 24, wherein the second alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer.

20 31. The semiconductor device according to Claim 22, further comprising a first well region of the second conductivity type connected electrically to the first electrode layer, the first well region covering the surface of the third alternating conductivity type layer on the side of the first major surface.

32. The semiconductor device according to Claim 24, further comprising a first well region of the second conductivity type connected electrically to the first electrode layer, the first well region covering the surface of the third alternating conductivity type layer on the side of the first major surface.

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33. The semiconductor device according to Claim 25, further comprising a second well region of the second conductivity type connected electrically to the first electrode layer, the second well region covering the surface of the extended portion of the second alternating conductivity type layer on the side of the first major surface.

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34. The semiconductor device according to Claim 26, further comprising a second well region of the second conductivity type connected electrically to the first electrode layer, the second well region covering the surface of the extended portion of the second alternating conductivity type layer on the side of the first major surface.

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35. The semiconductor device according to Claim 31, wherein the innermost second semiconductor region or the outermost second semiconductor region of the first alternating conductivity type layer in contact with the outermost fifth semiconductor region or the innermost fifth semiconductor region of the third alternating conductivity type layer is connected to the first well region of the second conductivity type.

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36. The semiconductor device according to Claim 32, wherein the innermost second semiconductor region or the outermost second semiconductor region of the first alternating conductivity type layer in contact with the outermost fifth semiconductor region or the innermost fifth semiconductor region of the third alternating conductivity type layer is connected to the first well region of the second conductivity type.

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37. The semiconductor device according to Claim 33, wherein the outermost second semiconductor region of the first alternating conductivity type layer in contact with the innermost third semiconductor region of the second alternating conductivity type layer is connected to the second well region of the second conductivity type.

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38. The semiconductor device according to Claim 34, wherein the outermost second semiconductor region of the first alternating conductivity type layer in contact with the innermost third semiconductor region of the second alternating conductivity type layer is connected to the second well region of the second conductivity type.

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39. The semiconductor device according to Claim 22, wherein the first peripheral portion of the first electrode layer is formed on a thick insulation film.

40. The semiconductor device according to Claim 24, wherein the first peripheral portion
15 of the first electrode layer is formed on a thick insulation film.

41. The semiconductor device according to Claim 25, wherein the second peripheral portion of the first electrode layer comprises a field plate.

20 42. The semiconductor device according to Claim 26, wherein the second peripheral portion of the first electrode layer comprises a field plate.

43. The semiconductor device according to Claim 22, wherein the first through sixth semiconductor regions of the first through third alternating conductivity type layer are shaped with respective stripes in a plane parallel to the first major surface or the second major surface.

5 44. The semiconductor device according to Claim 24, wherein the first through sixth semiconductor regions of the first through third alternating conductivity type layer are shaped with respective stripes in a plane parallel to the first major surface or the second major surface.

10 45. The semiconductor device according to Claim 43, wherein the pn-junctions in the second alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

15 46. The semiconductor device according to Claim 44, wherein the pn-junctions in the second alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

 47. The semiconductor device according to Claims 43, wherein the pn-junctions in the second alternating conductivity type layer extend in perpendicular to the pn-junctions in the first alternating conductivity type layer.

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 48. The semiconductor device according to Claims 44, wherein the pn-junctions in the second alternating conductivity type layer extend in perpendicular to the pn-junctions in the first alternating conductivity type layer.